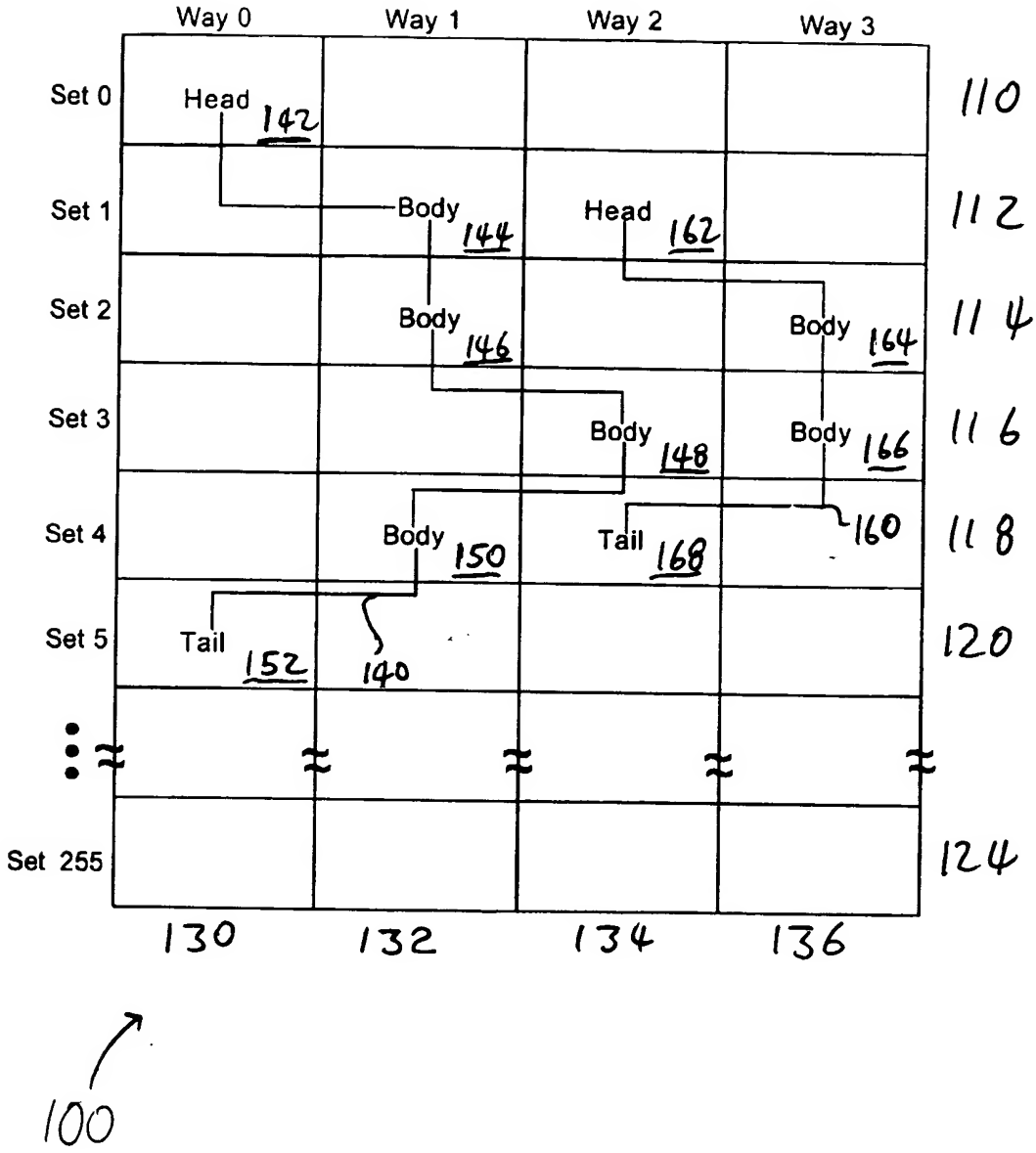
Way 0
Way 1
Way 2
Way 3
Set 0
Set 1
Set 2
Set 3
Set 4
Set 5
Set 255
Head 142
Body 144
Head 162
Body 146
Body 164
Body 148
Body 166
Body 150
Tail 168
160
Tail 152
140
110
112
114
116
118
120
124
130
132
134
136
100

FIGURE 1

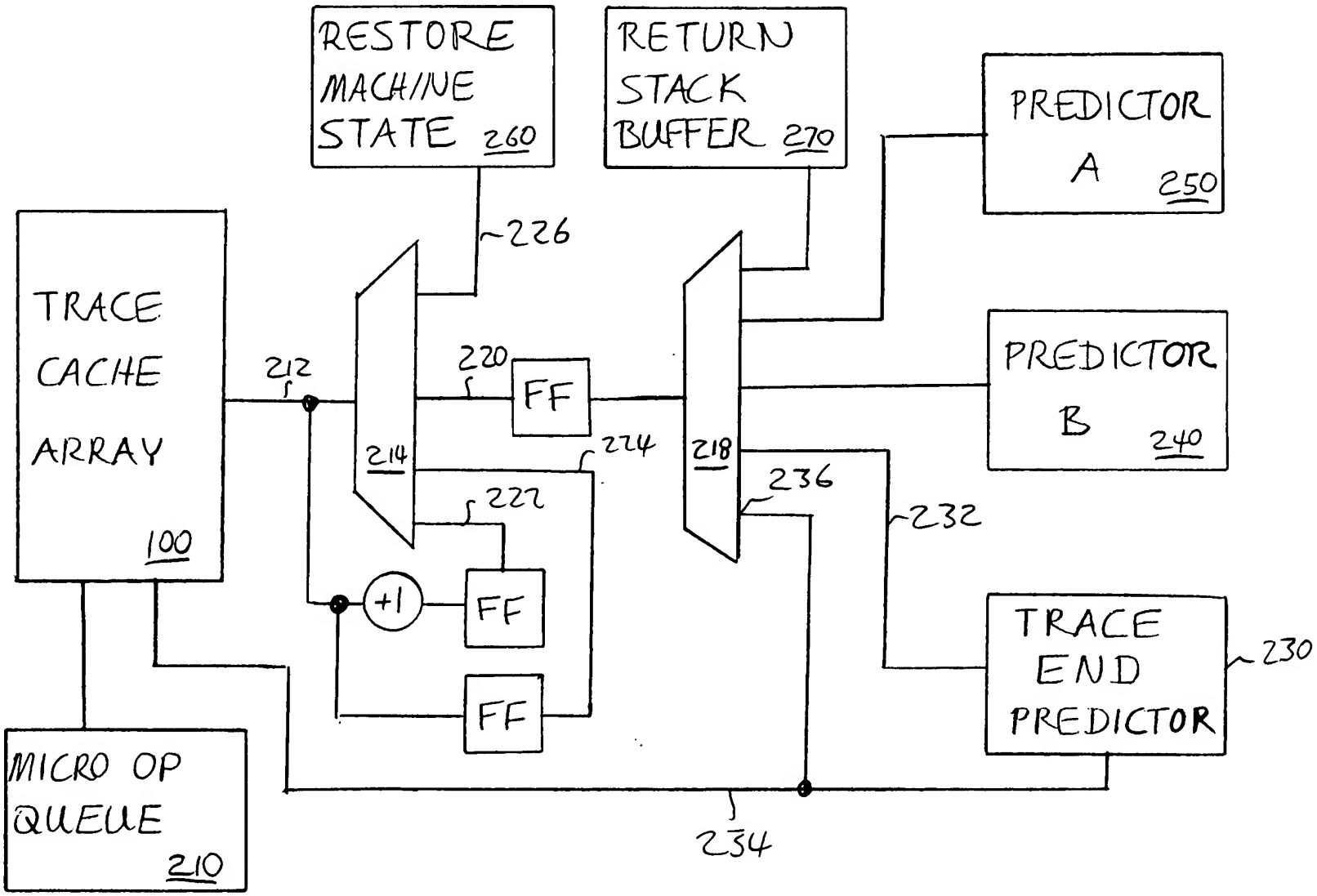
RESTORE MACHINE STATE 260
RETURN STACK BUFFER 270
PREDICTOR A 250
PREDICTOR B 240
TRACE CACHE ARRAY 100
226
212
220
FF
214
224
218
236
232
227
+1
FF
FF
TRACE END PREDICTOR
230
MICRO OP QUEUE 210
234

FIGURE 2

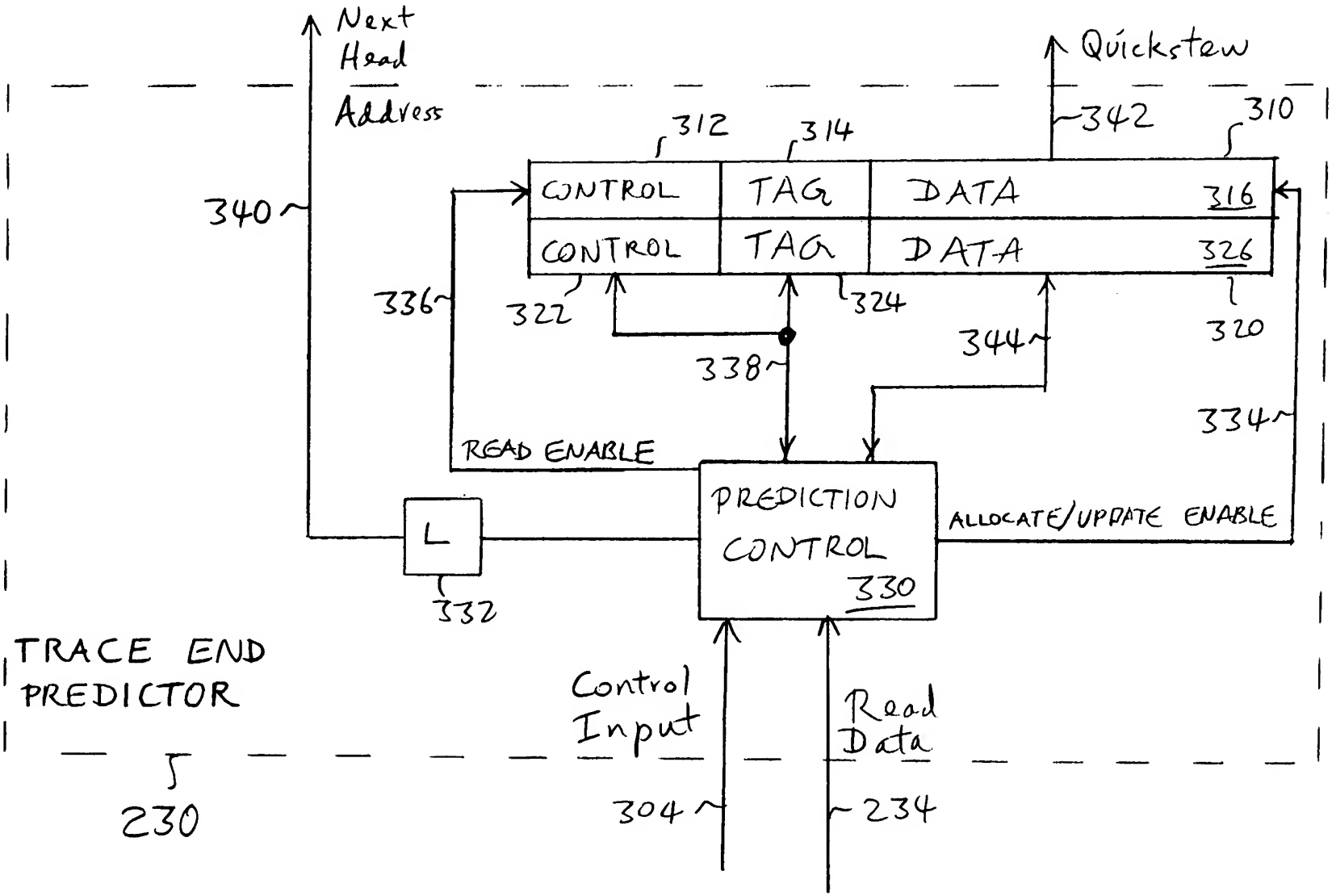
Next Head Address
Quickstew
342
310
312
314
CONTROL
TAG
DATA
316
CONTROL
TAG
DATA
326
340
336
322
324
320
344
338
334
READ ENABLE
PREDICTION CONTROL
330
ALLOCATE/UPDATE ENABLE
L
332
TRACE END PREDICTOR
230
Control Input
304
Read Data
234

FIGURE 3

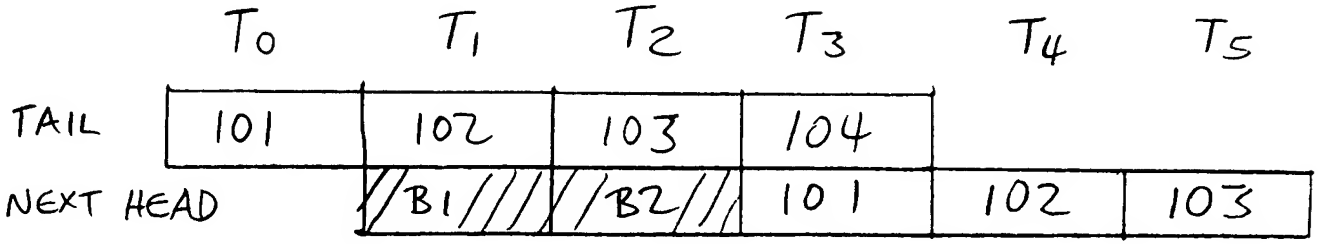

FIGURE 4A

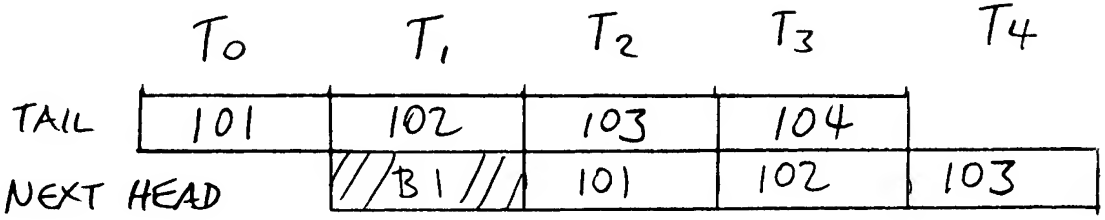

FIGURE 4B

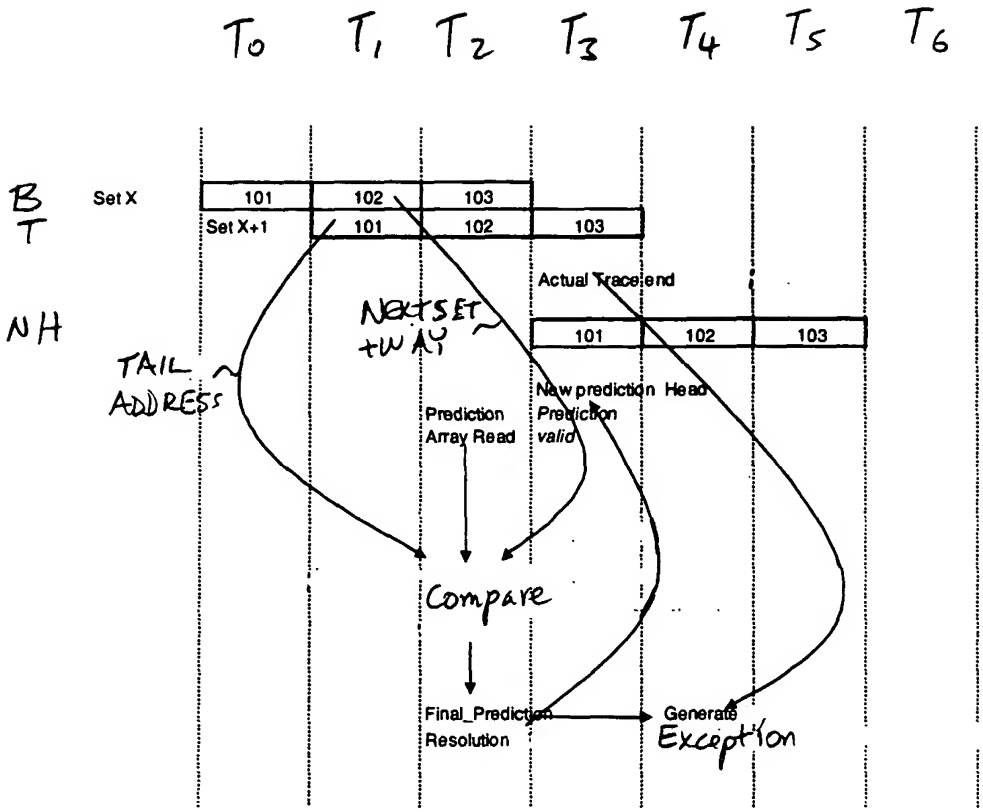
T0 T1 T2 T3 T4 T5 T6
BT
NH
Set X
Set X+1
101
102
103
101
102
103
Actual Trace end
NEXTSET +WAY
101
102
103
TAIL ADDRESS
Prediction Array Read
New prediction Head Prediction valid
Compare
Final_Prediction Resolution
Generate Exception

FIGURE 5

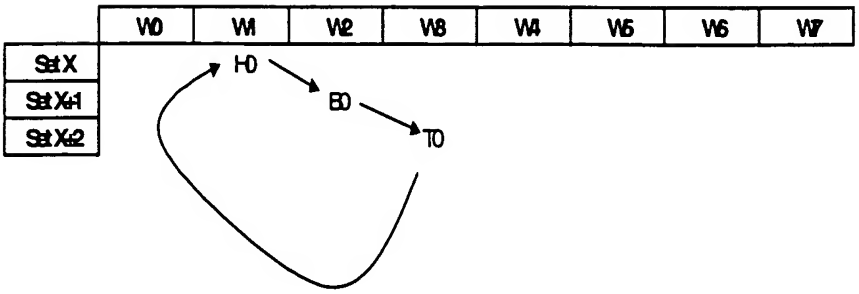

FIGURE 6A

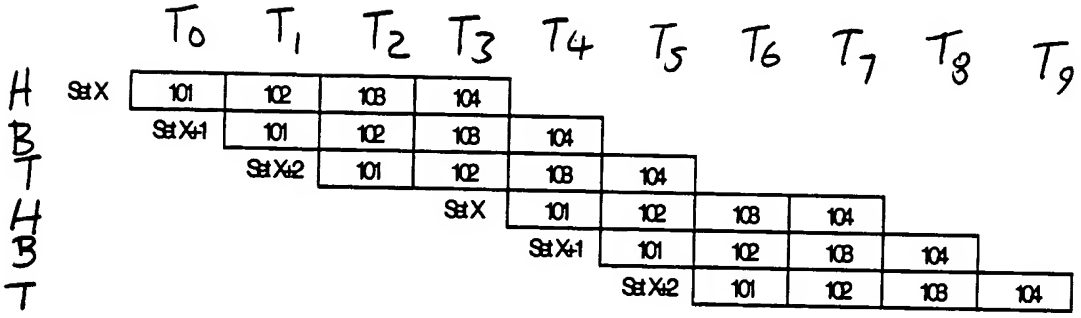

FIGURE 6B

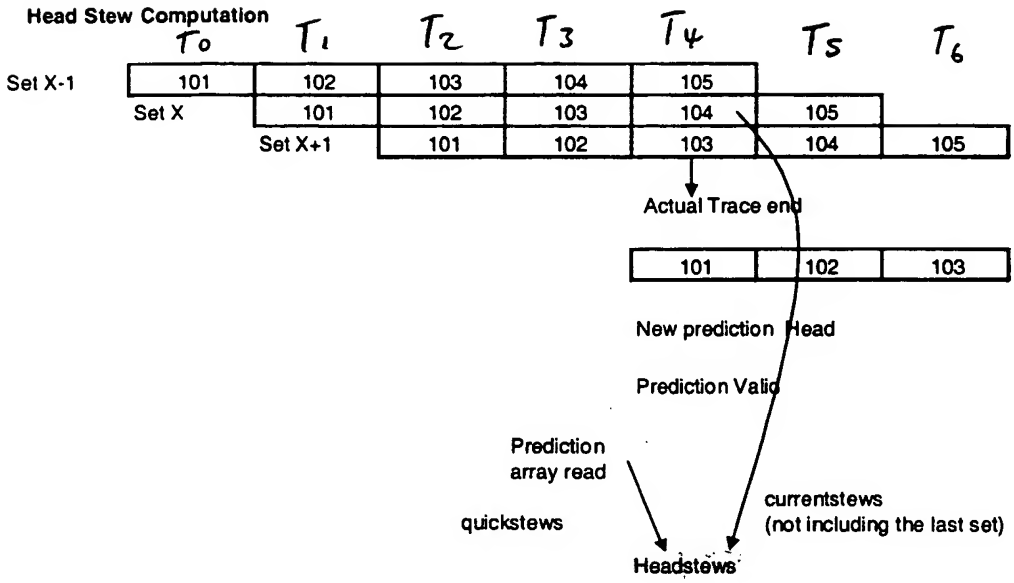
Head Stew Computation
T0
T1
T2
T3
T4
T5
T6
Set X-1
101
102
103
104
105
Set X
101
102
103
104
105
Set X+1
101
102
103
104
105
Actual Trace end
101
102
103
New prediction Head
Prediction Valid
Prediction array read
quickstews
currentstews (not including the last set)
Headstews

FIGURE 7

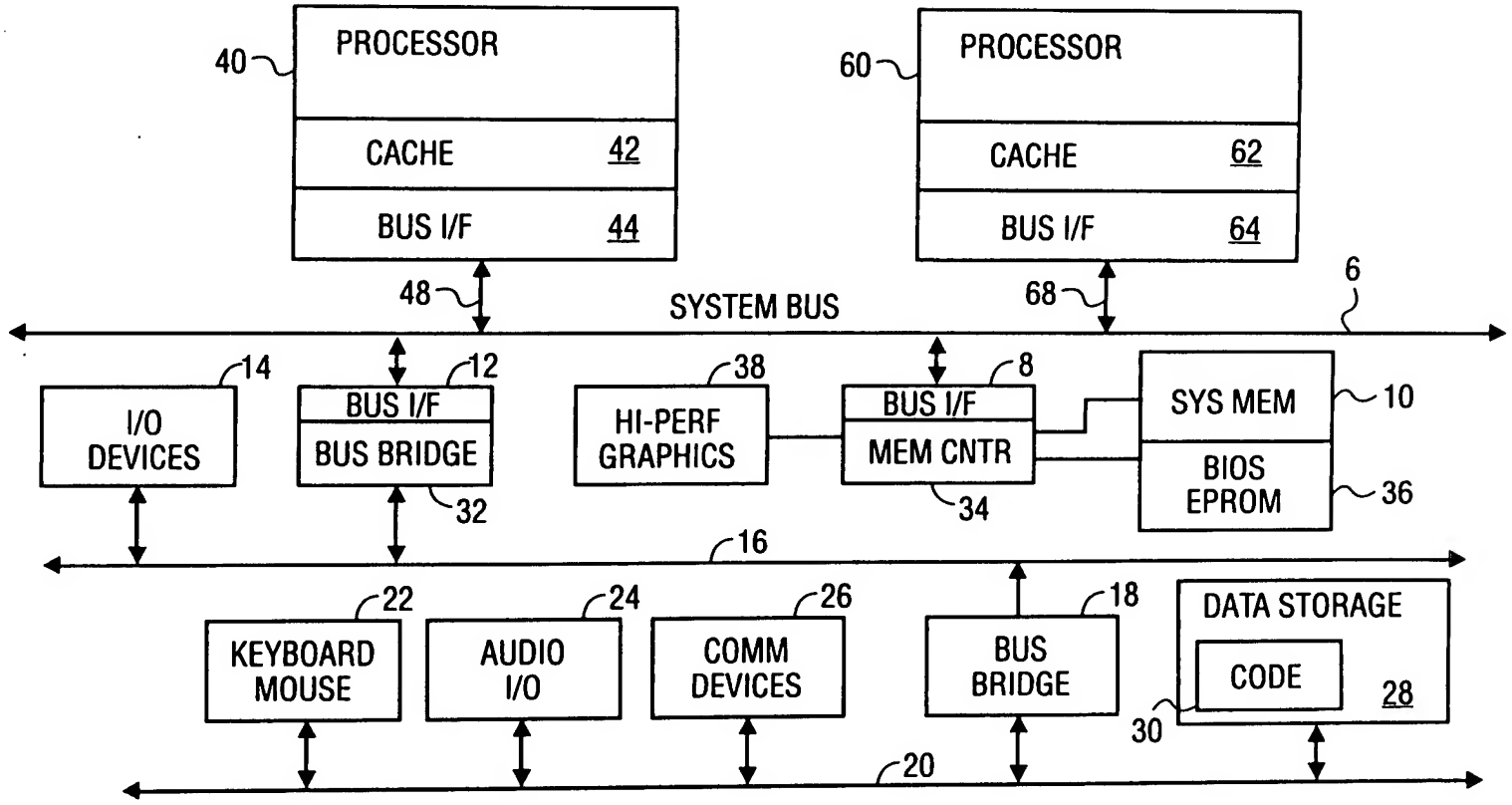
40
PROCESSOR
CACHE 42
BUS I/F 44
60
PROCESSOR
CACHE 62
BUS I/F 64
48
68
6
SYSTEM BUS
14
I/O DEVICES
12
BUS I/F
BUS BRIDGE
32
38
HI-PERF GRAPHICS
8
BUS I/F
MEM CNTR
34
SYS MEM
10
BIOS EPROM
36
16
22
KEYBOARD MOUSE
24
AUDIO I/O
26
COMM DEVICES
18
BUS BRIDGE
DATA STORAGE
CODE 28
30
20

FIG. 8